Transport Characteristics of Multichannel Transistors Made from Densely Aligned Sub-10 nm Half-Pitch Graphene Nanoribbons

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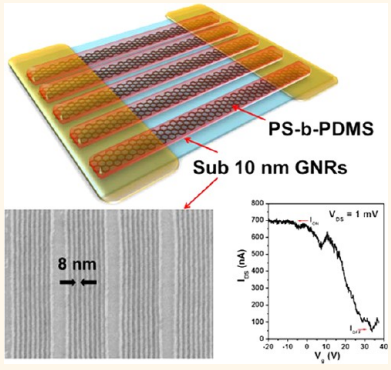
ABSTRACT Densely aligned sub-10 nm graphene nanoribbons are desirable for scale-up applications in nanoelectronics. We implemented directed self-assembly of block-copolymers in combination with nanoimprint lithography to pattern sub-10 nm half-pitch nanoribbons over large areas. These graphene nanoribbons have the highest density and uniformity to date. Multichannel field-effect transistors were made from such nanoribbons, and the transport characteristics of transistors were studied. Our work indicates that a large ribbon-to-ribbon width variation in a multichannel FET can lead to nonsynchronized switching characters of multiple graphene channels and thus a poor ON/OFF current ratio. Through process optimization, we have created 8 nm half-pitch graphene nanoribbons with the minimal ribbon-to-ribbon width variation of ~2.4 nm (3σ value). The corresponding transistors exhibit an ON/OFF current ratio >10, which is among the highest values ever reported for transistors consisting of densely arranged graphene nanoribbons. This work provides important insights for optimizing the uniformity and transport properties of lithographically patterned graphene nanostructures. In addition, the presented fabrication route could be further developed for the scalable nanomanufacturing of graphene-based nanoelectronic devices over large areas.



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One of the most exciting and pressing research directions of graphene is to examine how nanolithography technologies can be adapted, developed, and refined to pattern graphene sheets into nanostructures, in order to obtain desirable electronic characters and functionality that leverage the unique properties or potential of graphene.[1−5] A great amount of effort has been invested to produce graphene nanoribbons (GNRs) that have been experimentally demonstrated to be able to open an energy bandgap and hence enable semiconductor-related applications.[3,4,6] Moreover, recent work has also shown that graphene nanoribbons and other relevant nanostructures, once incorporated into nanoelectronic systems, exhibit different quantum transport behaviors than conventional semiconductor quantum devices (for example chaotic Dirac Billiard in Coulomb blockade,[7] Klein tunneling,[8] anomalous Hall effects,[9] and ballistic transport *via* metallic edge states of zigzag-edged GNRs.[10]) These newly identified properties may be further developed and employed in energy-efficient information systems, biosensors with low electronic noise, and energy conversion devices.

Although field effect transistors (FETs) based on single (or well isolated) sub-10 nm wide GNRs have been extensively studied, modern or break-through applications demand large arrays of densely arranged FETs.[4,11] To implement such scale-up applications, we need to develop multiplexing processes to create densely arranged arrays of sub-10 nm wide GNRs or other functional graphene nanostructures over large areas. Such spatially multiplexed graphene nanostructures, once incorporated into devices, can sustain a much higher driving current for electronic applications or ensure a high sensitivity for bio/chemical sensors. Recently, block copolymer (BCP) self-assembly has

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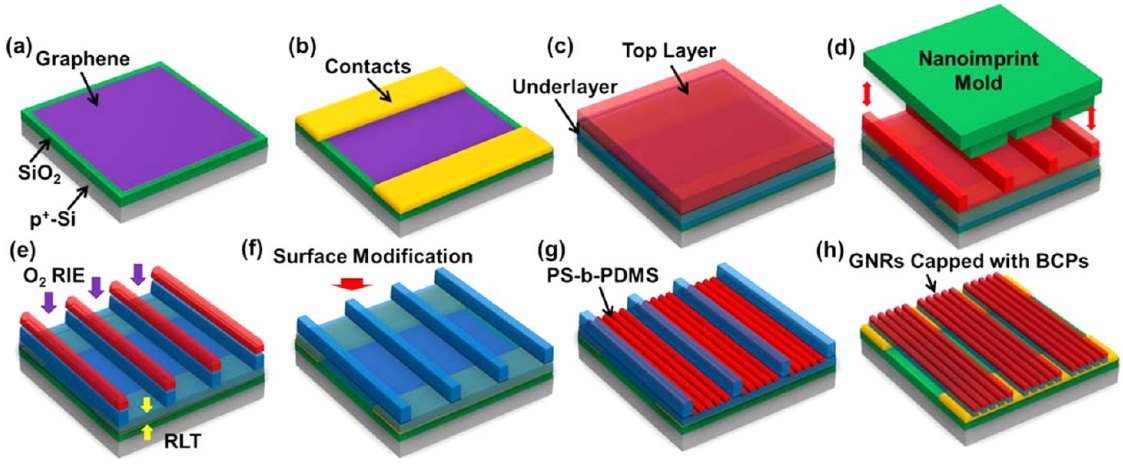

Figure 1. The fabrication route for patterning sub-10 nm half-pitch graphene nanoribbons using directed self-assembly of block copolymers: (a) deposition of the single-layer graphene; (b) fabrication of electrical contacts; (c) spin-coating of the underlayer (cross-linkable polymer) and the top layer (PMMA); (d) nanoimprinting of the top layer with directing nanostructures; (e) plasma etching for transferring the directing nanostructures into the underlayer and leaving a nonzero residual layer thickness (RLT); (f) surface modification of the underlayer after removing the residual PMMA; (g) directed self-assembly of PS-b-PDMS copolymer with cylindrical segregating morphology; and (h) plasma etching for patterning graphene nanoribbons using PDMS cylinders as the etching mask (here, overetching is performed to completely remove the directing structures and the underlying graphene, therefore preventing the formation of wide GNRs between the linear arrays of sub-10 nm GNRs).

been extensively studied as a promising lithographic technique for patterning sub-10 nm scale features densely aligned over large areas.[12−14] Several BCP-related methods have been developed to pattern graphene sheets into hexagonally packed graphene nanomeshes (GNMs) with sub-10 nm interhole spacing.[15−17] FETs based on GNMs exhibit a higher ON/OFF current ratio in comparison with FETs with unpatterned graphene channels, which indicates the formation of a bandgap in GNMs.[15,16] Such GNM-based transport channels can also carry a much larger driving current than a single GNR channel.[15,17] More recently, BCPs with cylindrical segregating morphology have been implemented to create graphene nanoribbons (GNRs) densely arranged over large areas.[18] For example, Dai *et al*. have created 35 nm pitch GNRs using BCP-based lithography.[18] GNR arrays can provide high scalability and uniformity for large-area electronic applications,[12] especially in making graphene-based transistors with scalable channel length.[19,20] In addition to BCP-based methods, other nanofabrication routes have been demonstrated to create densely aligned GNRs for scale-up applications. For example, Pan *et al*. demonstrated the fabrication of GNR arrays with a density of ~5 /μm through the wrinkle engineering.[21]

Further effort in this field aims to create narrower GNRs (*e.g.,* sub-10 nm width) to open a large bandgap and demonstrate a high ON/OFF current ratio in GNR-based FETs; pattern GNRs with the higher spatial density; and improve the degree of ordering and uniformity of GNRs over large areas for scale-up applications. Another critical and immediate challenge is that all recently reported ON/OFF current ratio (I_{ON}/I_{OFF}) data of FETs made from densely arranged graphene nanostructures (GNMs or GNRs) are typically less than 100,[15−18,21,22] and are far below the I_{ON}/I_{OFF} values obtained from the FETs consisting of single or well-isolated GNRs (*e.g.,* Wang *et al*. reported $I_{ON}/I_{OFF} \approx 10^6$ for a single GNR transistor).[11] To understand and identify underlying mechanisms for such a deterioration of ON/OFF current ratio due to the incorporation of multiple GNRs in a FET, the test-bed devices (*e.g.,* transistors) bearing densely aligned sub-10 nm GNRs are needed.

In this work, we studied the ON/OFF current characteristics of multi-GNR FETs as a function of ribbon-to-ribbon width variation (RWV) and ribbon width roughness (RWR). Here, the graphene sheets grown by chemical vapor deposition (CVD) were patterned into sub-10 nm half pitch GNRs by using directed self-assembly of cylindrical-morphology BCPs followed with plasma etching. Our work shows that the 3σ-RWV value among these densely arranged GNRs is strongly dependent on the processing condition of BCP self-assembly on top of graphene sheets, and it can significantly affect the overall ON/OFF current ratio of a FET with multiple GNR channels (N ≈ 50). A large RWV can lead to nonsynchronized switching characters of multi-GNR channels, and the FET becomes significantly leaky with a poor ON/OFF current ratio. To achieve a high ON/OFF current ratio of multi-GNR FETs, the ribbon-to-ribbon width variation needs to be minimized in the patterning process.

RESULTS AND DISCUSSION

Figure 1 schematically illustrates the fabrication route of sub-10 nm half-pitch (hp) graphene nanoribbons. First, a single-layer graphene sheet grown by chemical vapor deposition (CVD) is deposited onto a

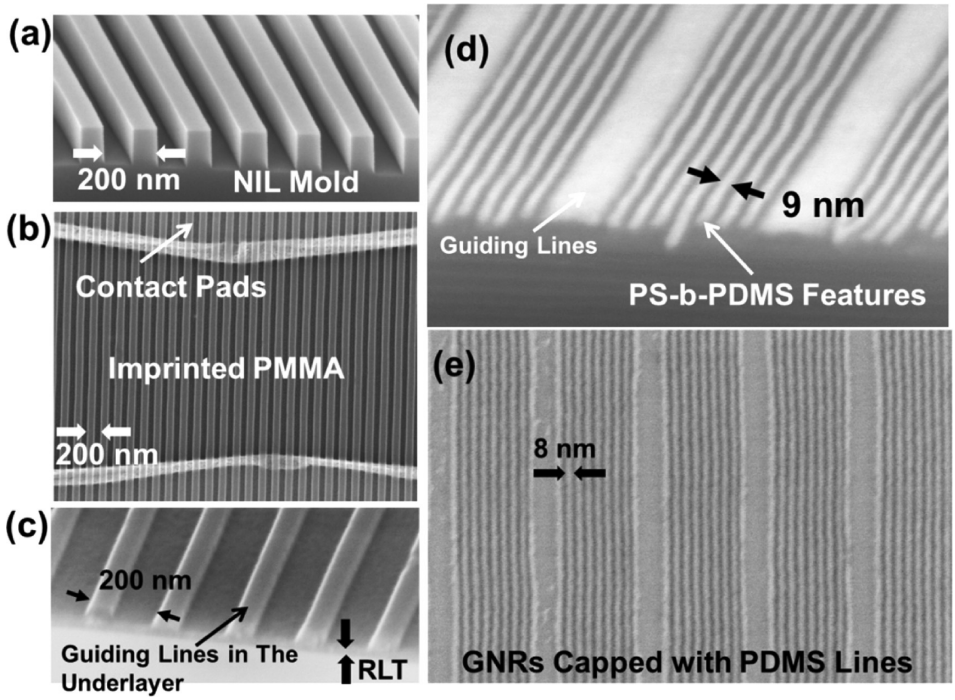

Figure 2. SEM images of (a) a Si mold bearing 200 nm period grating features; (b) 200 nm period gratings imprinted into the PMMA layer on top of stack of the underlayer, electrical contacts, and the graphene sheet; (c) 200 nm period gratings etched into the underlayer (cross-linked polymer), which serve as the directing features for directing the self-assembly of block copolymers; (d) well-oriented 9 nm half-pitch PDMS cylinders that were revealed from the segregated PS-*b*-PDMS film by O_2 plasma etching; and (e) 8 nm wide graphene nanoribbons patterned by a sequential plasma etching with the PDMS cylinders as the etching masks (note that the residual PDMS is still capped on top of graphene nanoribbons, and the directing features in the underlayer as well as underlying graphene have been completely removed by RIE).

Si/SiO_2 substrate (Figure 1a). The metal contact pads are then formed on top of the graphene sheet. This step is performed before any other fabrication processes to ensure a direct electrical contact to graphene devices for electronic characterization (Figure 1b). Afterward, two polymer layers were deposited on top of the graphene sheet in succession by spin-coating (Figure 1c). The underlayer is a thermally cross-linkable polymer, which, at the later steps, bears directing features and a grafted brush layer for the formation of ordered BCP patterns and also serves as an intermediate layer for transferring the BCP pattern into the underlying graphene. The top layer is a thermoplastic polymer suitable for thermal nanoimprint lithography.[23,24] A silicon mold is applied to imprint 200 nm period grating features into the top polymer layer through a thermal imprint cycle (Figure 1d). The imprinted grating pattern is subsequently etched into the cross-linked underlayer by O_2-based reactive ion etching (RIE) (Figure 1e). The RIE process is stopped before the underlayer is completely etched through, leaving a ~20 nm residual layer thickness (RLT) in the underlayer (Figure 1e). After completely removing the top-layer polymer in a solvent, the surface of the prestructured underlayer is modified by various brush layers and different grafting densities (Figure 1f). Afterward, a film of poly(styrene-*b*-dimethylsiloxane) (PS-*b*-PDMS) block copolymer is spun onto the prestructured underlayer, and then the sample is thermally annealed to induce the microphase separation of PS and PDMS domains in the copolymer (Figure 1g). During the phase separation, single-layer sub-10 nm hp PDMS cylinders are formed and aligned along the directing feature (*i.e.*, 200 nm pitch gratings) in the underlayer.[13] The PS domain is then selectively removed by a brief O_2-based plasma etching, leaving a monolayer of well-aligned PDMS cylinders on the underlayer, which can serve as the etching mask for subsequently etching the graphene sheet. Finally, directional CF_4/O_2-based RIE is performed to transfer the PDMS cylinder patterns into the cross-linked underlayer as well as the underlying graphene to form sub-10 nm hp graphene nanoribbons (Figure 1h). Here, it should be noted that over-etching is usually performed to completely remove the directing structures (*i.e.,* the protrusive lines in the underlayer) and underlying graphene, therefore preventing the formation of very wide GNRs between sub-10 nm GNRs.

The fabrication results of sub-10 nm GNRs have been observed by scanning electron microscopy (SEM) (Figure 2). Figure 2a shows the SEM image of a silicon mold bearing grating features with 200 nm period and 50% duty-cycle that were fabricated by using nanoimprint lithography (NIL) followed with anisotropic wet etching. Such a fabrication process has been demonstrated to be able to create ultrasmooth nanoimprinting

TABLE 1. Various Methods for Modifying the Surface of the Nanostructured Underlayer[a]

no.	surface modification to the underlayer[b]	average ribbon width () (nm)	3σ ribbon-to-ribbon width variation (RWV) (nm)	3σ ribbon width roughness (RWR) (nm)	correlation length of width roughness (ξ) (nm)
1	O_2 plasma etching	8.1	7.4	4.1	7.4
2	O_2 plasma etching + hydroxyl-terminated PS (PS−OH, 15 h[c])	8.6	6.0	3.8	7.1
3	O_2 plasma etching + 5 nm PECVD SiO_x + PS−OH, 0.5 h	7.6	5.1	3.6	7.0
4	O_2 plasma etching + 5 nm PECVD SiO_x + PS−OH, 2 h	7.8	4.3	3.7	6.8
5	O_2 plasma etching + 5 nm PECVD SiO_x + PS−OH, 8 h	8.7	3.8	3.7	7.0
6	O_2 plasma etching + 5 nm PECVD SiO_x + PS−OH, 15 h	8.0	2.4	3.5	6.7
7	O_2 plasma etching + 5 nm PECVD SiO_x + PDMS−OH, 15 h	8.8	3.0	4.0	6.8

[a] These methods result in significantly different values of ribbon-to-ribbon width variation (RWV) among multiple GNRs. However, the values of average ribbon width (), ribbon width roughness (RWR), and correlation length of width roughness (ξ) exhibit very weak dependence on the surface modification methods and conditions. [b] See the section of methods and materials for the processing details. [c] Annealing time for grafting PS−OH and PDMS−OH brush layers.

mold features precisely aligned to (111) crystallographic planes in (110)-oriented silicon.[25,26] This mold was used for imprinting directing features into the top polymer layer (*i.e.*, 100 nm thick poly(methyl methacrylate) (PMMA)). Figure 2b shows the SEM image of 200 nm grating features imprinted into the top PMMA layer, which was coated on top of a stack of the graphene, 50 nm thick Cr/Au electrode pads, and the underlayer (*i.e.*, 100 nm xHiRC antireflectance layer (ARC)). Figure 2b clearly shows that the step edges around the electrodes did not induce any damage or distortion of imprinted patterns. Such imprinted patterns in PMMA were subsequently transferred into the underlayer by O_2-based plasma etching. Figure 2c displays the cross-sectional SEM image of the underlayer etched with 200 nm period gratings (here the residual PMMA has been removed in toluene). It was noted that the pattern transfer from the PMMA to the underlayer caused a noticeable lateral etching of the protrusive lines and resulted in a reduced grating duty-cycle of ~28% (*i.e.*, 56/144 nm line/spacing). After pattern transfer, a ~20 nm residual layer thickness (RLT) is left in the underlayer in order to interface the copolymer patterns and the underlying graphene. Prior to the coating of PS-*b*-PDMS copolymers, the surface of the structured underlayer was modified to have high chain mobility and steric stabilization effects for the directed self-assembly of copolymer patterns.[13] Table 1 lists various surface modification methods we tested in this work. Figure 2d shows an exemplary SEM image of cylindrical-morphology PS-*b*-PDMS patterns formed on the structured underlayer that was treated by using method No. 6 in Table 1. Here, the PS domain has been removed by a brief O_2-based RIE, leaving 9 nm hp single-layer PDMS cylinders precisely aligned along the directing features in the underlayer. The PDMS pattern was finally transferred into the underlayer as well as the underlying graphene to form 8 nm hp graphene nanoribbons, as shown in the SEM image in Figure 2e. It is noted that in Figure 2e, all the protrusive directing features as well as the underlying graphene have been etched away, and no additional GNRs wider than 10 nm are formed between the linear arrays of sub-10 nm GNRs. For the GNR samples used for the transistor characterization, the PDMS cylinders are left on top of as-patterned GNRs, because (1) the cleaning process (*e.g.*, RCA or piranha methods) for eliminating such Si-contained cross-linked polymers can mechanically damage sub-10 nm scale graphene nanostructures (see Figure S1 in Supporting Information); (2) such PDMS cylinders may serve as an inertial cap for protecting as-patterned GNRs from external contamination.

To quantitatively evaluate the uniformity of as-patterned GNRs over a given sample substrate, we need to statistically measure ribbon width data from a number of GNRs. In this work, it is hard to directly measure the width of GNRs that are covered with PDMS cylinders. Here, we assume that the pattern of GNRs are faithfully replicated from the cylindrical-morphology of the single-layer PDMS domain in the copolymer, and thus the ribbon width can be reasonably approximated from the width data of PDMS cylinders after the final RIE process.

Figure 3 shows the critical steps to obtain statistical parameters for evaluating the uniformity of densely aligned GNRs. Figure 3a shows a typical high-resolution SEM image of as-etched PDMS cylinders on top of as-patterned GNRs. The edge profiles of multiple GNRs can be precisely extracted from such digitized SEM images by using a lab-made MATLAB program (Figure 3b), which is based upon Otsu's method that is widely used to automatically perform histogram shape-based image thresholding.[27] Here, the digitization definition is higher than 0.4 nm/pixel for all the SEM images. As demonstrated in Figure 3b, each of the ribbon profiles is indexed with a number (n). The mean width ($_n$) and the ribbon width roughness (RWR_n) of the nth GNR can be measured from the corresponding digitized profile. Here, $_n$ is simply the mean value of the ribbon width function ($w_n(z)$) along the nth GNR; RWR_n is defined as the standard deviation of $w_n(z)$ along the nth GNR. Figure 3c shows the width-correlation function $G_n(z)$ derived from the edge profile of the nth GNR by using eq 1 (for this example, $n = 3$; that is, Figure 3c plots the

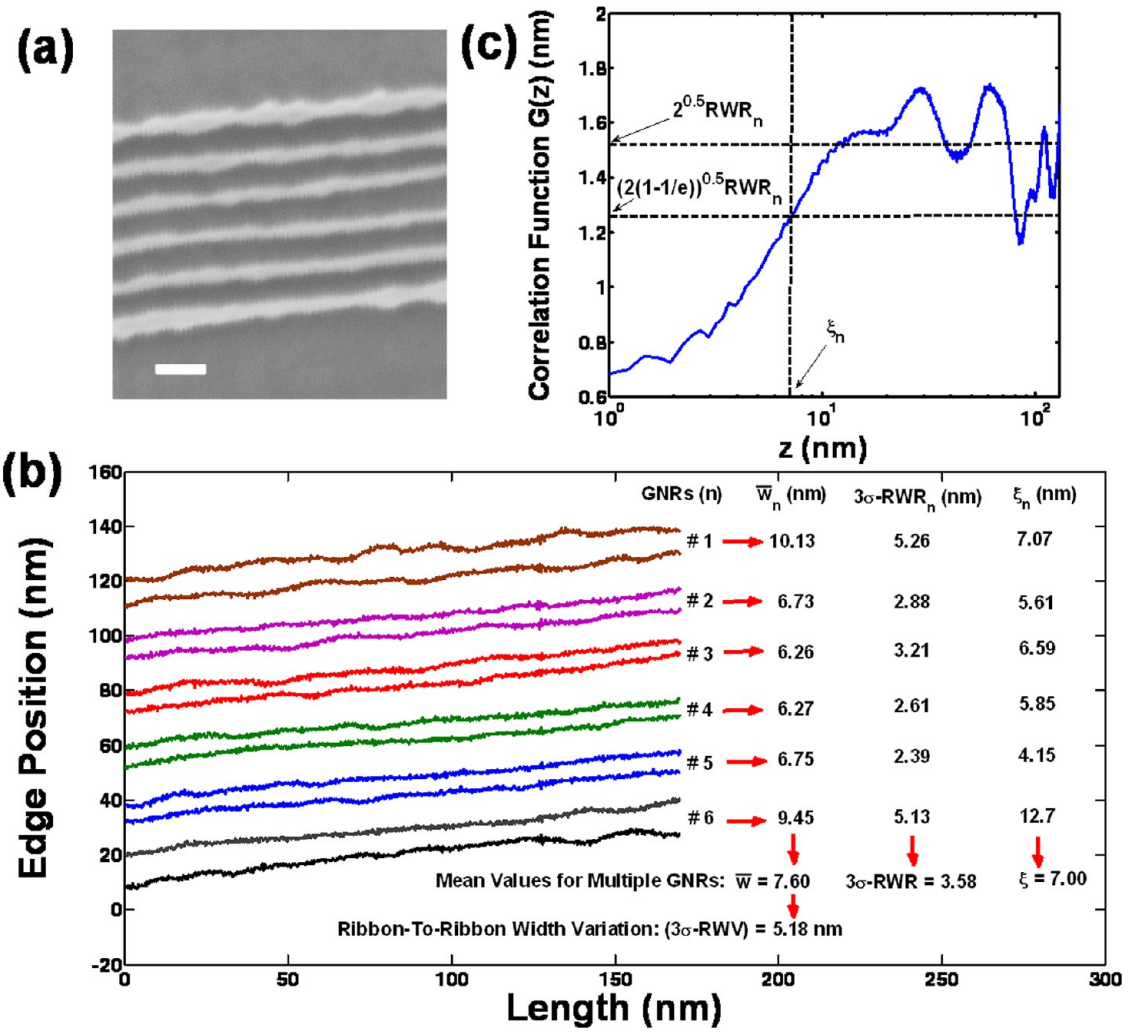

Figure 3. Measurement of ribbon-to-ribbon width variation (3σ-RWV) and ribbon width roughness (3σ-RWR) parameters of densely aligned GNRs. (a) High-resolution SEM image of as-etched PDMS cylinders on top of patterned GNRs (the scale bar is 20 nm). (b) The edge profiles of PDMS cylinders that are assumed to be the approximate profiles of underlying GNRs. Each GNR is indexed with a number (n). The mean width ($_n$), the ribbon width roughness (RWR$_n$), and the correlation length of width roughness (ξ_n) of the nth GNR are extracted from its digitized profile and accorded with a width-correlation function $G(z)$, as shown in panel c. w_n, RWR$_n$, and ξ_n are further statistically averaged to obtain the mean width (), the average ribbon width roughness (RWR), and the average correlation length of width roughness (ξ) of multiple GNRs (n = 1−50). In addition, ribbon-to-ribbon width variation (RWV) of multiple GNRs is calculated from the standard variance of $_n$ among multiple GNRs (n = 1−50).

width-correlation function of the third GNR shown in Figure 3b), where L is the length of imaged segments along GNRs.[28] The roughness correlation length (ξ_n) of the nth GNR can be extracted by letting G_n = (2(1 − 1/e))$^{0.5}$RWR$_n$, as demonstrated in Figure 3c.[28] Here, ξ_n is an important spatial roughness parameter for characterizing the spatial period of width fluctuation (or roughness) along a GNR.[28] Figure 3b lists $_n$, RWR$_n$, and ξ_n of all the GNRs shown in Figure 3a. The values of $_n$, RWR$_n$, and ξ_n are subsequently statistically averaged over multiple GNRs to obtain the mean width (), the average ribbon width roughness (RWR), and the average correlation length (ξ) of multiple densely aligned GNRs (it is noted that all the parameters without subscripts refer to the quantities averaged over multiple GNRs). In addition, ribbon-to-ribbon width variation (RWV) of multiple GNRs is defined from the standard deviation of $_n$ among multiple GNRs. It should be emphasized that RWV and RWR are two different parameters. RWV indicates the uniformity and dispersion of $_n$ among multiple GNRs (with different index n) on a sample substrate, as expressed by eq 2, whereas RWR measures the average degree of roughness (or width fluctuation) along the GNRs on a sample substrate, as expressed by eq 3. In eqs 2 and 3, N refers to the total sampling number of GNRs on a given sample substrate. In our analysis, N is larger than 50 for each sample.

$$G_n(z) = \left[\frac{1}{L-Z}\int_{s=0}^{s=L-Z}[w_n(S+Z) - w_n(S)]\,ds\right]^{1/2} \quad (1)$$

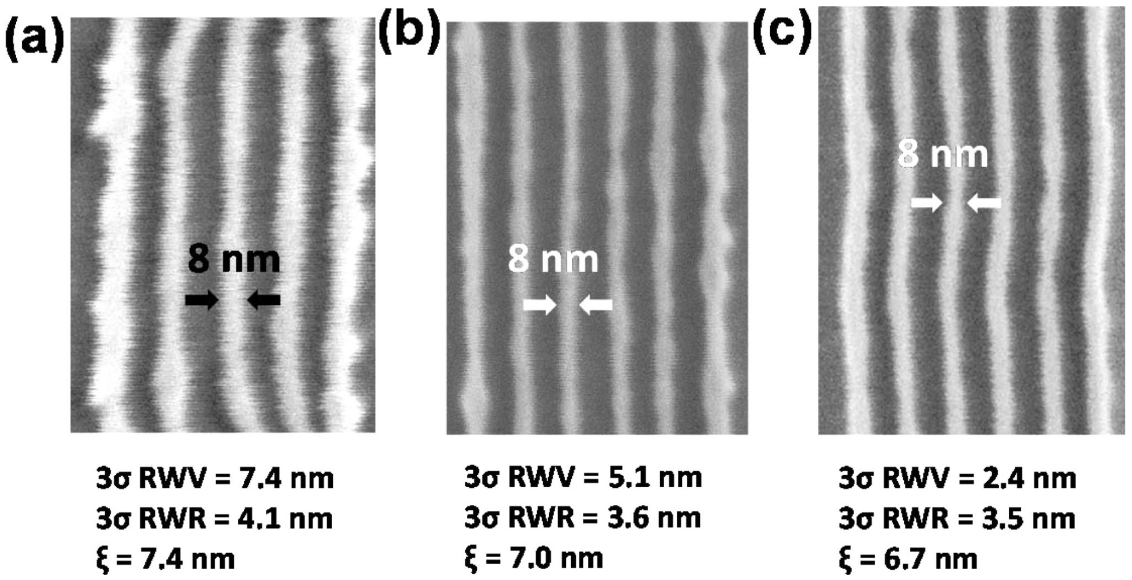

Figure 4. High-definition SEM images of 8 nm wide PDMS cylinders on top of patterned GNRs with ribbon-to-ribbon width variation (3σ-RWV) of (a) 7.4 nm, (b) 5.1 nm, and (c) 2.4 nm, which were caused by using different surface modification methods no. 1, 3, and 6, respectively (see Table 1). Each of the images is also labeled with corresponding values of ribbon width roughness (3σ-RWR) and correlation length of ribbon width roughness (ξ), which are much less sensitive to surface modification conditions. RWV and RWR are two different parameters. RWV is used for evaluating the overall uniformity of densely aligned GNRs in effective ribbon width ($_n$), whereas RWR represents the average degree of roughness along all GNRs, respectively.

$$\mathrm{RWV} = \sqrt{\frac{1}{N}\sum_{n=1}^{N}(\overline{w} - \overline{w}_n)^2} \qquad (2)$$

$$\mathrm{RWR} = \frac{\sum_{n=1}^{N} RWR_n}{N} \qquad (3)$$

In lithography technology, it is conventional to use 3σ values to evaluate the error in lithographically defined line width since nearly all possible width values lie within 3σ deviation of the mean width (). Here, all the RWV and RWR data are expressed by 3σ values.

Table 1 lists the data of $_n$, 3σ-RWV, 3σ-RWR, and ξ for GNR samples fabricated using various surface modification methods. The values of , 3σ-RWR, and ξ exhibit relatively weak dependence on the surface modification methods and conditions. This is because , 3σ-RWR, and ξ are mainly determined by the molecular weight and the Flory–Huggins parameter of PS-*b*-PDMS copolymers, and they are relatively independent of the grafting density of the brush layer.[29] However, the 3σ-RWV parameter (*i.e.*, ribbon-to-ribbon variation in average ribbon width $_n$ of individual GNRs) indeed exhibits a noticeable dependence on the surface modification methods. As shown in Table 1, the 3σ-RWV of various GNR samples ranges from 2.4 to 7.4 nm, which is strongly dependent on the processing conditions (*i.e.*, processing time and material choice) used for modifying the underlayer surface. Figure 4 displays the high-definition SEM images of three exemplary GNR samples fabricated by using surface modification methods (a) no. 1, (b) no. 3, and (c) no. 6, respectively, as listed in Table 1. These three GNR samples have quite close values of (~8 nm), 3σ-RWR (3.5–4.1 nm), and ξ (6.7–7.4 nm), whereas they exhibit significantly different values of 3σ-RWV: (a) 7.4 nm, (b) 5.1 nm, and (c) 2.4 nm. Jung *et al*. previously reported that the variation of solvent annealing conditions as well as the surface modification methods (*i.e.*, no brush, PS-brush, and PDMS-brush) for the self-assembly of PS-*b*-PDMS can strongly affect the morphological uniformity and ordering of BCP microdomains over large areas.[29] Here, we further demonstrated that the variation of surface processing times of brush layers also plays an important role in determining the uniformity of the cylindrical BCP features. The different processing durations of the brush layers are expected to result in different grafting densities of the brush molecules. A low grafting density can cause the low diffusivity of the polymer on the surface, leading to nonequilibrium morphologies and hence nonuniform BCP patterns.[30]

During the nanofabrication process, we *in situ* measured the transport characteristic curves of back-gated graphene-based field-effect transistors (FETs) to monitor the evolution of ON/OFF characteristics of processed graphene at different fabrication phases (i.e., unpatterned pristine graphene, graphene coated with polymer films, as-imprinted samples, thermal annealing of BCPs, and as-etched GNRs) and subsequently investigate the effect of RWV and RWR parameters on the ultimate transport properties of densely aligned GNRs. Figure 5a shows the drain/source current (I_{DS})–gate voltage (V_G) characteristic curve of a control FET made from unpatterned monolayer graphene (channel

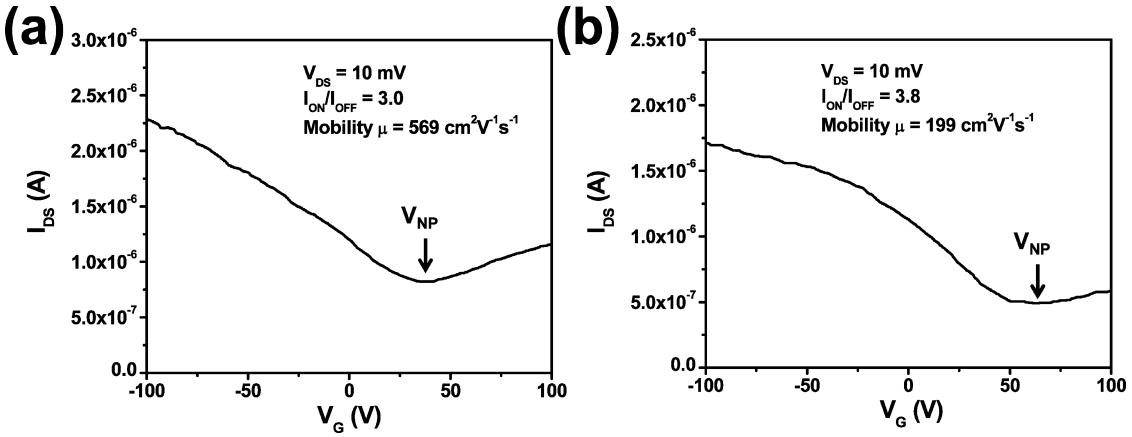

Figure 5. $I_{DS}-V_G$ characteristic curves of (a) a control FET just made from unpatterned pristine graphene and (b) the same control device coated with polymer layers.

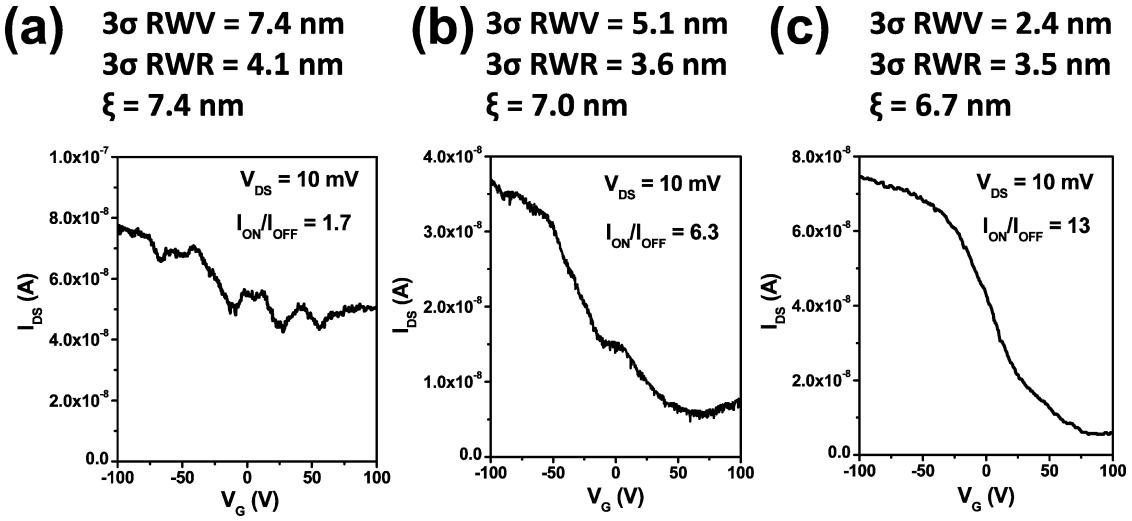

Figure 6. $I_{DS}-V_G$ characteristic curves of three exemplary multichannel FETs with ribbon-to-ribbon width variation (3σ-RWV) of 7.4 nm (a), 5.1 nm (b), and 2.4 nm (c).

width, 5 μm; channel length, 10 μm; and gate dielectric thickness, 300 nm), which exhibits a typical ambipolar transport behavior and a relatively low ON/OFF current ratio ($I_{ON}/I_{OFF} \approx 3.0$). The hole mobility of this FET was measured to be 569 $cm^2\ V^{-1}\ s^{-1}$. For all 11 control FETs fabricated in the same batch, ON/OFF ratios range from 2.2 to 4.0 (or $I_{ON}/I_{OFF} = 3.0 \pm 0.7$) and mobility values were measured to be $862 \pm 240\ cm^2\ V^{-1}\ s^{-1}$. Figure 5b shows the $I_{DS}-V_G$ characteristic curve of the same exemplary control FET after being coated with the polymer layers (*i.e.*, the cross-linked underlayer and the plastic top layer illustrated in Figure 1c). The polymer coating resulted in a noticeable shift of the electric charge neutrality point (V_{NP}) from 36 to 64 V that is attributed to the additional electrostatic doping brought by the polymer layers. After the polymer coating, the mobility of this FET was reduced to 199 $cm^2\ V^{-1}\ s^{-1}$ and the ON/OFF ratio was slightly increased to 3.8. For all 11 polymer-coated control FETs, the mobility values were reduced to $287 \pm 81\ cm^2\ V^{-1}\ s^{-1}$ and ON/OFF ratios were statistically measured to be 3.4 ± 0.5, that is also slightly higher than those of original control FETs without polymer coating. The reason for such an increase of the ON/OFF ratio due to the polymer coating is still unknown. The nanoimprint process and the thermal annealing of BCPs did not induce noticeable change of the transport characteristics of graphene FETs (not shown here). This may be because that both of these two processes were not directly applied to the graphene channel.

After the plasma etching using aligned PS-*b*-PDMS domains as the etching mask, we finally fabricated back-gated FETs consisting of multiple GNR channels (the total number (N) of GNR channels in a FET is about 50). Figure 6 displays $I_{DS}-V_G$ characteristic curves of three exemplary multichannel FETs, which were made from GNR samples shown in Figure 4. As mentioned above, the GNR arrays in these FETs have very close values of average ribbon width ($w \approx 8$ nm), average ribbon width roughness (3σ-RWR: 3.5−4.1 nm), and average roughness correlation length (ξ: 6.7−7.4 nm), but significantly different values of ribbon-to-ribbon

width variation (*i.e.*, 3σ-RWV: (a) 7.4 nm, (b) 5.1 nm, and (c) 2.4 nm). In comparison with the control device, the GNR-based FETs exhibit two distinct features: (1) The electrical transport is dominated by the hole conductance, which has been widely observed in graphene nanoelectronic structures etched by O_2-based plasma and has been attributed to the oxidation to the edges of GNRs.[11,16,31] (2) The overall ON/OFF current ratio (I_{ON}/I_{OFF}) of a FET is sensitive to 3σ-RWV values of multiple active GNRs in the FET. In particular, the FET with 3σ-RWV of 7.4 nm (Figure 6a) exhibits a relatively poor ON/OFF current ratio ($I_{ON}/I_{OFF} \approx 1.7$) that is even lower than that of the control FET with unpatterned graphene (*i.e.*, $I_{ON}/I_{OFF} = 3.0 \pm 0.7$). In addition, multiple irregular conduction minima were typically observed on the $I_{DS}-V_G$ curve. With decreasing RWV value (*i.e.*, increasing the ribbon-to-ribbon uniformity in ribbon width), the total number of discrete conduction minima is reduced and the ON/OFF current ratio of the FETs is noticeably enhanced. The exemplary FET in Figure 6b has 3σ-RWV of 5.1 nm and $I_{ON}/I_{OFF} \approx 6.3$. There are a total of nine multi-GNR FETs with 3σ-RWV of ~5.1 nm that were fabricated in the same batch using the same surface modification method. ON/OFF ratios of these 9 FETs are statistically measured to be in the range of 4–6.9 (statistical mean value, 5.2; standard deviation, 1.4), which are statistically higher than the I_{ON}/I_{OFF} values of control FETs with unpatterned graphene (*i.e.*, 3.0 ± 0.7). Figure 6c shows the $I_{DS}-V_G$ curve of one of the FETs with the smallest 3σ-RWV (~2.4 nm) in this work, which exhibits a higher ON/OFF current ratio ($I_{ON}/I_{OFF} \approx 13$). There are a total of 11 multi-GNR FETs with 3σ-RWV of 2.4 nm that were fabricated in the same batch. The transport characteristic curves of all of these FETs are listed in the Supporting Information (see Figure S2). The ON/OFF ratios of these 11 FETs are statistically measured to be in the range of 6–16 (statistical mean value, 11; standard deviation, 3.5). This mean value of I_{ON}/I_{OFF} is among one of the highest I_{ON}/I_{OFF} values reported for transistors made from densely aligned graphene nanoribbons.[18,21]

In Figure 7, ON/OFF ratio data of all multichannel FETs are respectively plotted as functions of (a) 3σ-RWV and (b) 3σ-RWR parameters. Each of solid squares shown in Figure 7 refers to the statistical mean value of ON/OFF ratio data acquired from 9–12 FETs that were fabricated using a given surface modification method listed in Table 1 and hence have the same RWV and RWV values. The error bars indicate the standard deviations. It is clearly shown that the ON/OFF ratios of multi-GNR FETs are more correlated to RWV rather than RWR. Figure 7a suggested that in order to achieve a high ON/OFF current ratio well above 10, 3σ-RWV of incorporated GNRs needs to be at least smaller than 2 nm.

It is a very important finding that a relatively large ribbon-to-ribbon variation of average ribbon widths can result in a poor ON/OFF current ratio for a FET with

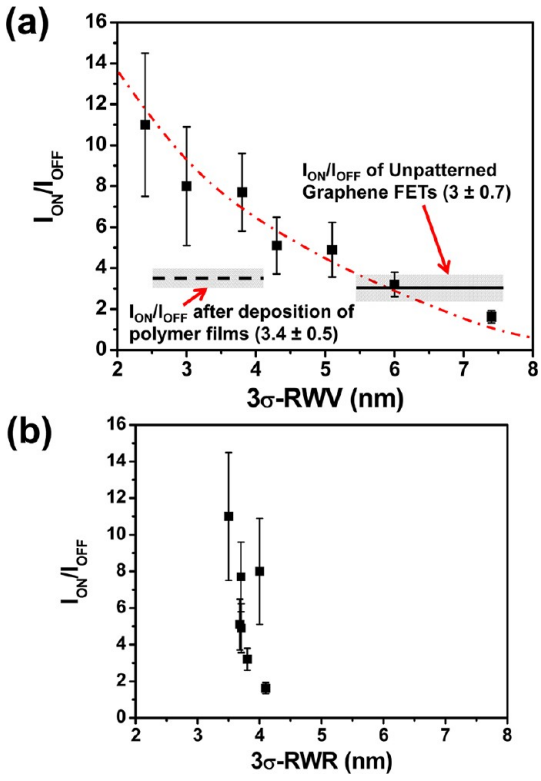

Figure 7. ON/OFF current ratio data (solid squares) of FETs consisting of multiple parallel GNR channels ($N \approx 50$) plotted as a function of (a) ribbon-to-ribbon width variation (3σ-RWV) and (b) ribbon width roughness (3σ-RWR). Here, each of the solid squares is the mean value of ON/OFF ratio data statistically measured from 9–12 FETs that were fabricated under the same processing conditions and have the same value of 3σ-RWV and 3σ-RWR. The error bars measure the standard deviations. In panel a, the horizontal solid line indicates the average ON/OFF ratio of the control FETs made from unpatterned pristine graphene. The vertical thickness of the shaded area attached to the solid line represents the standard deviation of ON/OFF ratio data of all the control FETs. The dashed line with shaded area indicates the ON/OFF ratio data of the FETs after deposition of multiple polymer layers.

multiple GNRs. This phenomenon can be qualitatively explained by the nonsynchronization of OFF states of multiple nonuniform GNRs. The large variation of ribbon width among multiple GNRs could lead to a significantly different magnitude of quantum confinement of carriers, doping from edges, and voltages corresponding to the electric charge neutrality point (V_{NP}) for each of the GNR channels.[20] Once these nonuniform GNRs are integrated together in a single FET, the multiple GNR channels cannot simultaneously reach the conductance minima at the same gate voltage. In such a case, the transistor becomes very leaky with a poor ON/OFF current ratio and usually exhibits multiple irregular conduction minima on the $I_{DS}-V_G$ curves, which is attributed to the superposition of $I_{DS}-V_G$ curves of multiple GNRs with different electric charge neutrality points (V_{NP}). Although the previous simulation work done by Yoon *et al.* suggests that the ribbon edge roughness may significantly

affect the ON/OFF ratio of GNR-based transistors,[32] the present work experimentally demonstrates that RWV is indeed the most critical factor leading to the nonuniformity of transport properties of GNRs and thus poor ON/OFF ratios of multichannel transistors.

In addition to the ON/OFF current characteristics, the carrier mobility (μ) data of multichannel FETs were also extracted from $I_{DS}-V_G$ characteristic curves by using eq 4 (valid for the linear region of GNR-based FETs), where C_{GNR} is the average gate capacitance associated with a single nanoribbon per unit channel length [unit: F/m]; L is the channel length; N is the number of GNR channels involved in a multichannel FET.[33] Here, C_{GNR} is calculated by using a simulation model based on finite element analysis (FEA) that takes into account the fringe effect at the ribbon edges, as shown in Figure S3 in the Supporting Information. The curve slope value (or transconductance $\Delta I_{DS}/\Delta V_G$) at the linear region of an $I_{DS}-V_G$ characteristic curve can be obtained by the linear fitting, as denoted by the red line in Figure 8a. Figure 8b only plots the mobility data (solid squares) of the multichannel FETs with 3σ-RWV values less than 4.5 nm. For the FETs with 3σ-RWV > 4.5 nm, multiple irregular conduction minima appear on their $I_{ds}-V_g$ curves, which makes it very difficult to obtain a well-defined transconductance. As a comparison, Figure 8b also shows the average mobility of control FETs with unpatterned pristine graphene (indicated by the upper solid line) and that of the same batch of FETs coated with polymer layers (indicated by the lower solid line). As discussed above, the coating of polymer layers reduces the hole mobility in unpatterned graphene from 862 ± 240 to 287 ± 81 cm^2/(V s). The nanoimprint process and the thermal annealing of BCPs did not induce a noticeable change of the mobility of graphene channels (not shown in Figure 8b). The most noticeable reduction of mobility occurs when the graphene film is etched into densely aligned GNRs. As shown in Figure 8b, all the multi-GNR FETs exhibit a mobility that is 1 order of magnitude lower than that of polymer-coated control FETs, which is attributed to significantly increased scattering magnitude of carriers at the ribbon-edge roughness. Figure 8b also shows that the carrier mobility of multi-GNR FETs only weakly depends on RWV. This is probably because of that the carrier mobility may be mainly determined by the scattering at ribbon-edge roughness (or ribbon-width roughness (RWR)) that is not significantly modulated in this work, as shown in Table 1. So far the highest mobility of our multichannel FETs is measured to be ~25 cm^2/(V s).

$$\mu = \frac{\Delta I_{DS}}{N C_{GNR} \frac{1}{L} V_{DS} \Delta V_G} \quad (4)$$

On the basis of our experimental observation and analysis, it is suggested that the RWV and RWR values of densely aligned GNRs needs to be minimized in the patterning process in order to achieve a high ON/OFF current ratio as well as high carrier mobility in multi-GNR FETs. We have improved the ON/OFF current ratio of multichannel FETs up to an order of magnitude of 10 through the optimization of the processing conditions for the directed self-assembly of BCPs. However, these I_{ON}/I_{OFF} values are still far below previously reported I_{ON}/I_{OFF} values of single-GNR FETs with the similar average ribbon width (*e.g.*, $I_{ON}/I_{OFF} \approx 200$ for a 9 nm wide single-GNR FETs).[3,4] The future work will aim to develop technologies able to further improve the uniformity of GNRs and etch pristine graphene nanostructures with well-controlled edge morphologies, which is expected to greatly improve the transport properties of multi-GNR FETs.

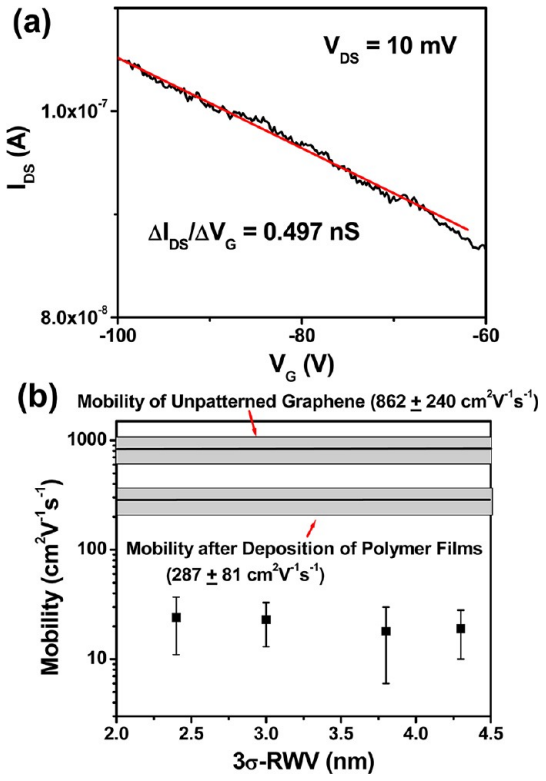

Figure 8. (a) Extraction of the transconductance ($\Delta I_{DS}/\Delta V_G$) through fitting the linear region of the $I_{DS}-V_G$ characteristic curve of a multi-GNR FET. (b) Carrier mobility data (solid squares) of multi-GNR FETs plotted as a function of ribbon-to-ribbon width variation (3σ-RWV). Here, each of the solid squares is the mean value of mobility data statistically acquired from 9−12 FETs that were fabricated under the same processing conditions and have the same value of 3σ-RWV. The error bars measure the standard deviations. In panel b, the horizontal solid lines indicate the average mobility of FETs with unpatterned pristine graphene (upper line: μ = 862 ± 240 cm^2/(V s)) and the same batch of FETs after deposition of polymer layers (bottom line: μ = 287 ± 81 cm^2/(V s)). The vertical thickness of shaded boxes represents the corresponding standard deviation of mobility data.

CONCLUSION

We patterned sub-10 nm half-pitch graphene nanoribbons and fabricated field-effect transistors bearing

such densely arranged GNRs. The nanofabrication method combines nanoimprint lithography and directed self-assembly of block copolymers. Our work shows that the standard deviation of the average ribbon width among densely arranged GNRs strongly depends on the processing conditions of BCP self-assembly, and it can significantly affect the ON/OFF current characteristics of the FETs bearing multiple GNR channels. A relatively large ribbon-to-ribbon width variation (RWV) of multiple GNRs can result in a poor ON/OFF current ratio, which is attributed to the nonsynchronization of OFF states of multiple nonuniform GNRs. Through process optimization, we are able to create 8 nm hp GNRs with width RWV less than 3 nm (3σ value). The FET bearing ~50 such GNRs exhibits a relatively high ON/OFF current ratio >10, which is well above that of the control FET with an unpatterned graphene channel and is also among the highest values ever reported for transistors bearing densely arranged graphene nanoribbons. Our work provides important scientific insights for understanding the mechanism responsible for the deterioration of ON/OFF current characteristics of graphene-based FETs when incorporated with multiple GNR channels. In addition, the nanofabrication method and the device structure presented in this work could be further developed to realize the massive production of high-quality graphene nanostructures for future scale-up electronic applications.

METHODS AND MATERIALS

Graphenes, Substrates, and Electrodes. The CVD-grown graphene monolayers on the Cu foils were purchased from Graphene-Supermarket, Inc. and transferred onto 300 nm thick SiO_2/p^+-Si substrates by using a graphene-transferring kit (also from Graphene-Supermarket, Inc.). To form drain/source electrodes of multichannel FETs, 55 nm thick Cr/Au contact pads were made onto the graphene by using photolithography, metal evaporation, and lift-off in a solvent. The total transistor channel width is 2 μm, within which there are approximately 50 parallel sub-10 nm wide graphene nanoribbons electrically connecting the drain and the source electrodes. The total channel length is 10 μm.

Fabrication of Directing Structures in the Underlayers. The underlayer uses xHiRC antireflectance coating (ARC) polymer (Brewer Science), which was deposited on the graphene sheet by spin-coating followed with 20 min of thermal annealing at 180 °C. The final thickness was measured to be 40 nm. The top polymer layer for nanoimprint lithography is 100 nm thick polymethylmethacrylate (PMMA) (molecular weight of 25K) that is spin-casted from 3 wt % solution in toluene. The Si mold for imprinting 200 nm period grating features (duty cycle, 50%; feature depth, 130 nm) was replicated from a master mold (Nanonex, Inc.) by using nanoimprint lithography followed with anisotropic wet etching. The thermal imprint process was performed on a Specac thermal pressing system equipped with a cooling-water system. The imprint process was performed at 120 °C under a gauge pressure of 1.4 MPa. The as-imprinted patterns in the top layer (PMMA) were transferred into the underlayer by O_2-based RIE (O_2 flow rate, 10 sccm; pressure, 20 mTorr; power, 90 W; etching rate, ~60 nm/min). The film thickness as well as the etching rate was measured by using an ellipsometer.

Surface Modification of the Underlayers. In some experiments, the surfaces of nanostructured underlayers were modified by hydroxyl-terminated poly(styrene) (PS−OH) or poly(dimethylsiloxane) (PDMS−OH) homopolymers with a molecular weight 5 kg/mol (Polymer Source, Inc.), which were spin-coated on the underlayer and then annealed at 150 °C for a time duration ranging from 0.5 to 15 h (see Table 1). For the surface modification methods no. 3−7 listed in Table 1, prior to the grafting of the brush layers, the underlayer was coated with 5 nm thick SiO_x by plasma-enhanced chemical vapor deposition (PECVD) at 250 °C.

Directed Self-Assembly of Block-Copolymers. The block-copolymer used for patterning sub-10 nm graphene nanoribbons is polystyrene-*block*-polydimethylsiloxane (PS-*b*-PDMS, $M_{n,PS}$ = 11 kg/mol and $M_{n,PDMS}$ = 5 kg/mol) (Polymer Source, Inc.) with cylindrical segregating morphology. The PS-*b*-PDMS patterns were formed onto the substrate by spin-coating of 0.9 wt % solution in toluene followed with 180 °C thermal annealing for 5 h.

Plasma Etching To Form Sub-10 nm Wide Graphene Nanoribbons. To reveal 9 nm half-pitch PDMS cylinders aligned in the PS matrix and then to transfer the PDMS pattern into the underlying graphene, the PS-*b*-PDMS film was subjected to a sequential plasma etch including CF_4-based RIE (CF_4 flow rate, 20 sccm; pressure, 10 mTorr; RF power, 50 W; time duration, 3 s) to remove the PDMS surface layer, O_2-based RIE (O_2 flow rate, 10 sccm; pressure, 20 mTorr; RF power, 90 W; time duration, 10 s) to remove the PS matrix, CF_4-based plasma again (CF_4 flow rate, 20 sccm; pressure, 10 mTorr; RF power, 90 W; time duration, 3 s) to etch through PECVD SiO_x, and O_2-based RIE again (O_2 flow rate, 10 sccm; pressure, 10 mTorr; RF power, 90 W; time duration, 35 s) to directionally etch the underlayer as well as the underly graphene. The patterned BCPs and graphene nanoribbons were imaged by using a FEI Nova Nanolab SEM.

Transistor Characterization. The fabricated FETs bearing multiple GNRs were characterized at room temperature by using an Agilent 4145B semiconductor analyzer connected to a probe station.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Sub-10 nm wide graphene nanoribbons revealed by removing residual PDMS and underlayer materials; all multi-GNR FETs with 3σ-RWV of 2.4 nm fabricated using surface modification method no. 6 in the same batch; finite element analysis for simulating electric field around densely aligned graphene nanoribbons and calculating effective gate capacitance associated with nanoribbons (C_{GNR}). This material is available free of charge *via* the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

1. Geim, A. K. Graphene: Status and Prospects. *Science* **2009**, *324*, 1530–1534.

2. Son, Y. W.; Cohen, M. L.; Louie, S. G. Half-Metallic Graphene Nanoribbons. *Nature* **2006**, *444*, 347–349.
3. Han, M. Y.; Özyilmaz, B.; Zhang, Y. B.; Kim, P. Energy Band-Gap Engineering of Graphene Nanoribbons. *Phys. Rev. Lett.* **2007**, *98*, 206805/1–206805/4.
4. Li, X. L.; Wang, X. R.; Zhang, L.; Lee, S.; Dai, H. J. Chemically Derived Ultrasmooth Graphene Nanoribbon Semiconductors. *Science* **2008**, *319*, 1229–1232.
5. Tapasztó, L.; Dobrik, G.; Lambin, P.; Biró, L. P. Tailoring the Atomic Structure of Graphene Nanoribbons by Scanning Tunneling Microscope Lithography. *Nat. Nanotechnol.* **2008**, *3*, 397–401.
6. Lin, Y. M.; Perebeinos, V.; Chen, Z. H.; Avouris, P. Electrical Observation of Subband Formation in Graphene Nanoribbons. *Phys. Rev. B* **2008**, *78*, 161409/1–161409/4.
7. Ponomarenko, L. A.; Schedin, F.; Katsnelson, M. I.; Yang, R.; Hill, E. W.; Novoselov, K. S.; Geim, A. K. Chaotic Dirac Billiard in Graphene Quantum Dots. *Science* **2008**, *320*, 356–358.
8. Young, A. F.; Kim, P. Quantum Interference and Klein Tunneling in Graphene Heterojunctions. *Nat. Phys.* **2009**, *5*, 222–226.
9. Gusynin, V. P.; Sharapov, S. G. Unconventional Integer Quantum Hall Effect in Graphene. *Phys. Rev. Lett.* **2005**, *95*, 146801/1–146801/4.
10. Wang, X. R.; Ouyang, Y. J.; Jiao, L. Y.; Wang, H. L.; Xie, L. M.; Wu, J.; Guo, J.; Dai, H. J. Graphene Nanoribbons with Smooth Edges Behave as Quantum Wires. *Nat. Nanotechnol.* **2011**, *6*, 563–567.
11. Wang, X. R.; Ouyang, Y. J.; Li, X. L.; Wang, H. L.; Guo, J.; Dai, H. J. Room-Temperature All-Semiconducting Sub-10 nm Graphene Nanoribbon Field-Effect Transistors. *Phys. Rev. Lett.* **2008**, *100*, 206803/1–206803/4.
12. Park, S.; Lee, D. H.; Xu, J.; Kim, B.; Hong, S. W.; Jeong, U.; Xu, T.; Russell, T. P. Macroscopic 10-Terabit-per-Square-Inch Arrays from Block Copolymers with Lateral Order. *Science* **2009**, *323*, 1030–1033.
13. Jung, Y. S.; Lee, J. H.; Lee, J. Y.; Ross, C. A. Fabrication of Diverse Metallic Nanowire Arrays Based on Block Copolymer Self-Assembly. *Nano Lett.* **2010**, *10*, 3722–3726.
14. Park, S. M.; Liang, X. G.; Harteneck, B. D.; Pick, T. E.; Hiroshiba, N.; Wu, Y.; Helms, B. A.; Olynick, D. L. Sub-10 nm Nanofabrication *via* Nanoimprint Directed Self-Assembly of Block Copolymers. *ACS Nano* **2011**, *5*, 8523–8531.
15. Bai, J.; Zhong, X.; Jiang, S.; Huang, Y.; Duan, X. Graphene Nanomesh. *Nat. Nanotechnol* **2010**, *5*, 190–194.
16. Liang, X. G.; Jung, Y. S.; Wu, S. W.; Ismach, A.; Olynick, D. L.; Cabrini, S.; Bokor, J. Formation of Bandgap and Subbands in Graphene Nanomeshes with Sub-10 nm Ribbon Width Fabricated *via* Nanoimprint Lithography. *Nano Lett.* **2010**, *10*, 2454–2460.
17. Kim, M.; Safron, N. S.; Han, E.; Arnold, M. S.; Gopalan, P. Fabrication and Characterization of Large-Area Semiconducting Nanoperforated Graphene Materials. *Nano Lett.* **2010**, *10*, 1125–1131.
18. Jiao, L. Y.; Xie, L. M.; Dai, H. J. Densely Aligned Graphene Nanoribbons at ~35 nm Pitch. *Nano Res.* **2012**, *5*, 292–296.
19. Areshkin, D. A.; White, C. T. Building Blocks for Integrated Graphene Circuits. *Nano Lett.* **2007**, *7*, 3253–3259.
20. Castro Neto, A. H.; Guinea, F.; Peres, N. M. R.; Novoselov, K. S.; Geim, A. K. The Electronic Properties of Graphene. *Rev. Mod. Phys.* **2009**, *81*, 109–162.
21. Pan, Z. H.; Liu, N.; Fu, L.; Liu, Z. F. Wrinkle Engineering: A New Approach to Massive Graphene Nanoribbon Arrays. *J. Am. Chem. Soc.* **2011**, *133*, 17578–17581.
22. Liang, X.; Jung, Y.-S.; Wu, S.; Ismach, A.; Olynick, D. L.; Cabrini, S.; Bokor, J., Graphene Nanomeshes with Sub-10 nm Ribbon Width Fabricated *via* Nanoimprint Lithography in Combination with Block Copolymer Self-Assembly. *Proc. Int. Conf. on Electron, Ion, Photon Beam Technol. Nanofabr.* **2010**, *7C, Nanoelectronics*, 7C/1–7C/2.
23. Chou, S. Y.; Krauss, P. R.; Renstrom, P. J. Imprint of Sub-25 nm Vias and Trenches in Polymers. *Appl. Phys. Lett.* **1995**, *67*, 3114–3116.
24. Chou, S. Y.; Krauss, P. R.; Renstrom, P. J. Imprint Lithography with 25-Nanometer Resolution. *Science* **1996**, *272*, 85–87.
25. Yu, Z. N.; Chen, L.; Wu, W.; Ge, H. X.; Chou, S. Y. Fabrication of Nanoscale Gratings with Reduced Line Edge Roughness Using Nanoimprint Lithography. *J. Vac. Sci. Technol., B* **2003**, *21*, 2089–2092.
26. Liang, X. G.; Morton, K. J.; Austin, R. H.; Chou, S. Y. Single Sub-20 nm Wide, Centimeter-Long Nanofluidic Channel Fabricated by Novel Nanoimprint Mold Fabrication and Direct Imprinting. *Nano Lett.* **2007**, *7*, 3774–3780.
27. Otsu, N.; Thresholding, A Selection Method from Gray-Level Histograms. *IEEE Trans. Syst., Man, Cybern.* **1979**, *9*, 62–66.
28. Constantoudis, V.; Patsis, G. P.; Tserepi, A.; Gogolides, E. Quantification of Line-Edge Roughness of Photoresists. II. Scaling and Fractal Analysis and the Best Roughness Descriptors. *J. Vac. Sci. Technol., B* **2003**, *21*, 1019–1026.
29. Jung, Y. S.; Ross, C. A. Orientation-Controlled Self-Assembled Nanolithography Using a Polystyrene−Polydimethylsiloxane Block Copolymer. *Nano Lett.* **2007**, *7*, 2046–2050.
30. Harrison, C.; Chaikin, P. M.; Huse, D. A.; Register, R. A.; Adamson, D. H.; Daniel, A.; Huang, E.; Mansky, P.; Russell, T. P.; Hawker, C. J.; *et al.* Reducing Substrate Pinning of Block Copolymer Microdomains with a Buffer Layer of Polymer Brushes. *Macromolecules* **2000**, *33*, 857–865.
31. Wang, X. R.; Li, X. L.; Zhang, L.; Yoon, Y.; Weber, P. K.; Wang, H. L.; Guo, J.; Dai, H. J. N-Doping of Graphene through Electrothermal Reactions with Ammonia. *Science* **2009**, *324*, 768–771.
32. Yoon, Y.; Guo, J. Effect of Edge Roughness in Graphene Nanoribbon Transistors. *Appl. Phys. Lett.* **2007**, *91*, 073103/1–073103/3.
33. Muller, R. S.; Kamins, T. I.; Chan, M. *Device Electronics for Integrated Circuits*, 3rd ed.; John Wiley & Sons: New York, 2002; pp 431−432.